REMARKS

Reconsideration of the application, in view of the following remarks is respectfully requested.

The examiner rejects Claim 24 under 35 U.S.C. § 103(a) as being unpatentable over Watson et al in view Sevenhans et al. The examiner states that with regard to Claim 24 Watson et al discloses a successive approximation apparatus in Fig. 3 but does not explicatively disclose a SAR ADC that comprises a single multi-bit ADC coupled to the output of the amplifier. The examiner states that Sevenhans et al discloses a system in Fig. 1 that comprises a single ADC that is coupled to an output of an amplifier A2 that converts the amplified signal. The examiner states that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Watson et al.'s system with that of Sevenhans et al in order to remove offset from an input signal being input thereto.

This rejection is respectfully traversed. The examiner has specifically pointed to Col. 5, lines 55-63 of Sevenhans et al. This portion of the reference points out the examiner's error in making the combination. This paragraph recites:

> "Still another characteristic feature of the present direct conversion receiver is that said additional correction circuit includes a comparator comparing said difference signal with zero and thereby acting as a one-bit analog-to-digital convertor, cascaded..." (emphasis added).

Although the examiner states that the device comprises a single ADC, Claim 24 recites "a single multi-bit analog to digital convertor" (emphasis added). In view of the fact that Sevenhans et al teaches a one bit ADC and Watson et al teaches a one bit ADC, it is clear that the combination would have a one-bit ADC, not the multi-bit ADC referred to by the examiner and specifically recited in the claim. Accordingly, Claim 24 is clearly distinguished over this combination of the references and no changes to the claim are necessary to provide an allowable claim, and thus none have been made.

The examiner rejects Claims 2-11, 13-23 under 35 U.S.C. § 103(a) as being unpatentable over Watson et al. in view Sevenhans et al. as applied to claim 24 and further in view of Burns.

In view of the above discussion concerning the combination of Watson et al with Sevenhans et al, adding Burns to the group of references to reject the present application does not change the fact that the rejection must fail because only a one-bit ADC can be contemplated.

The examiner rejects Claim 18 under 35 § U.S.C. 102(b) as being anticipated by Watson et al. The examiner specifically refers to Fig. 3. As previously stated, Watson utilizes a separate analog to digital convertor 24 for each bit in the conversion. In Watson, the comparator makes a comparison between the conversion between the input signal to a digital signal and then back to an analog signal, amplifies the difference and then passes it on to the next stage. Therefore, one ADC is required for each bit resolution.

In sharp contrast, in the present invention only utilizes a single multi-bit ADC which functions as a comparator until the amplified difference signal is within the range of the ADC, thus reutilizing the same circuitry for generating all of the bits.

Accordingly, Applicants believe that the application is in condition for allowance and such action is respectfully requested.

Respectfully submitted,
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